**1)**

**ANS**

Prediction Accuracy = (14/18) x 100

= 77.77 %

|  | **12** | **18** | **23** | **40** | **42** | **44** | **46** | **48** | **50** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **B1 Buffer** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **B1 Predicted** | Not  Taken | Not  Taken | Not  Taken | Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken |
| **B1 Predictor** | Correct | Correct | Incorrect | Incorrect | Correct | Correct | Correct | Correct | Correct |
| **B2 Buffer** | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| **B2 Predicted** | Taken | Taken | Taken | Not  Taken | Taken | Taken | Taken | Taken | Taken |
| **B2 Predictor** | Correct | Correct | Incorrect | Incorrect | Correct | Correct | Correct | Correct | Correct |

**2)**

**ANS**

Prediction Accuracy = (15/18) x 100

= 83.33 %

|  | **12** | **18** | **23** | **40** | **42** | **44** | **46** | **48** | **50** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **B1 Buffer** | 10 | 00 | 00 | 01 | 00 | 00 | 00 | 00 | 00 |
| **B1 Predicted** | Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken | Not  Taken |
| **B1 Predictor** | Incorrect | Correct | Incorrect | Correct | Correct | Correct | Correct | Correct | Correct |
| **B2 Buffer** | 10 | 11 | 10 | 11 | 11 | 11 | 11 | 11 | 11 |
| **B2 Predicted** | Taken | Taken | Taken | Taken | Taken | Taken | Taken | Taken | Taken |
| **B2 Predictor** | Correct | Correct | Incorrect | Correct | Correct | Correct | Correct | Correct | Correct |

**3)**

**ANS**

Prediction Accuracy = (97/99) x 100

= 97.97 %

| **Iteration** | **2-bit** | **Comment** | **Correctness** |
| --- | --- | --- | --- |
| 1st | 0 | Not Taken | Incorrect |
| 2nd to 98 | 1 | Taken | Correct |
| 99 | 1 | Taken | Incorrect |

**4)**

**ANS**

Prediction Accuracy = (96/99) x 100

= 96.96 %

| **Iteration** | **2-bit** | **Comment** | **Correctness** |
| --- | --- | --- | --- |
| 1st | 00 | Not Taken | Incorrect |
| 2nd | 01 | Taken | Incorrect |
| 3rd to 98 | 11 | Taken | Correct |
| Last | 10 | Taken | Incorrect |

**5)**

**ANS**

| **aa=3, bb=2** | **Branch** |
| --- | --- |
| 01,01,01 | L1,L2,L3  Prediction |
| Incorrect | L1 Not Taken |
| Correct | L2 Not Taken |
| Correct | L3 Not Taken |

| **aa=4, bb=5** | **Branch** |
| --- | --- |
| 11,00,11 | L1,L2,L3  Prediction |
| Correct | L1 Taken |
| Incorrect | L2 Not Taken |
| Incorrect | L3 Taken |

| **aa=2, bb=2** | **Branch** |
| --- | --- |
| 11,01,11 | L1,L2,L3  Prediction |
| Incorrect | L1 taken |
| Correct | L2 Not Taken |
| Correct | L3 Taken |

**6)**

**ANS**

| **Branch Address** | **Predicted PC** | **Predicted Taken bits** |
| --- | --- | --- |
| 2012 | 2020 | 1 |
| 2036 | 2064 | 1 |

| **Branch Address** | **Predicted PC** | **Predicted Taken bits** |
| --- | --- | --- |
| 2012 | 2020 | 1 |
| 2024 | 2032 | 1 |
| 2036 | 2064 | 1 |

**7)**

**ANS**

a) Commit the register by writing F2 then remove instruction from ROB

b) Commit the register by writing F2 then remove instruction from ROB

c) Commit 0(R2) register by writing it and then remove instruction from ROB

d) Commit R3 register and then remove instruction from ROB

e) Remove instruction from ROB

**8)**

**ANS**

Loop: fld f2,0(Rx) =>1+3

I0: fmul.d f2,f0,f2 =>1+4

I1: fdiv.d f8,f2,f0 =>1+10

I2: fld f4,0(Ry) =>1+3

I3: fadd.d f4,f0,f4 =>1+2

I4: fadd.d f10,f8,f2 =>1+2

I5: fsd f4,0(Ry) =>1+1

I6: addi Rx,Rx,8 =>1+0

I7: addi Ry,Ry,8 =>1+0

I8: sub x20,x4,Rx =>1+0

I9: bnz x20,Loop =>1+1

Number of cycles per loop iteration = 37

**9)**

**ANS.**

Resulting rewritten code:

Loop: LD t9,0(Rx)

I0: MULTD t10, f0, f2

I1: DIVD t11, t9, t10

I2: LD t12, 0(Ry)

I3: ADDD t13, f0, t12

I4: SUBD t14, t11, t13

I5: SD t14, 0(Ry)